REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-7 remain in the application. Claim 1 has been amended.

In the section entitled "Drawings" on page 2 of the above-identified Office action, the drawings have been objected to because the Examiner has stated that in FIG. 3 the drawing should demonstrate that the spacers 12 are formed in the trench before the polysilicon layer 11 is deposited therein.

Applicants believe that FIG. 3 is correct. As clearly described on page 10, line 23 to page 11, line 2 of the specification, the production of the additional spacers 12 before the deposition of the polysilicon is only an alternative embodiment. The sidewall spacers 12 can be provided or not. It is clear from the comparison of FIGs. 3 and 4 what the subsequent intermediate product looks like in the case of the embodiment according to FIG. 4.

The Examiner is, therefore, requested to withdraw the objection to the drawings.

In the section entitled "Claim Rejections - 35 USC § 102" on pages 2-8 of the above-mentioned Office action, claims 1-7 have been rejected as being anticipated by Palm et al. (US 6,548,861 B2) under 35 U.S.C. § 102(e).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references. However, the language of claim 1 has been modified to correct a typographical error.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer, a storage layer, and an upper boundary layer;
>
> forming an oxide region in each case on a side of the doped regions remote from the semiconductor body, the oxide region being thicker than the lower boundary layer;
>
> before the upper boundary layer is applied and after the application of the storage layer, applying a sacrificial layer made from a material selectively etchable with respect to a material of the storage layer and to polysilicon onto the storage layer;
>
> producing openings in the sacrificial layer, the storage layer, and the lower boundary layer, extending to the semiconductor body, by using a mask.

Claim 4 calls for, inter alia:

> applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric and including a lower boundary layer, a storage layer, and an upper boundary layer; and
>
> forming an oxide region thicker than the lower boundary layer, in each case, on a side of the doped region remote from the semiconductor body;
>
> before producing the upper boundary layer and after the application of the storage layer, applying a sacrificial layer with a topside to the storage layer;
>
> producing openings with lateral walls in the sacrificial layer, the storage layer, and the lower boundary layer, by using a mask;
>
> introducing dopant into implantation regions of the semiconductor body through the openings;
>
> etching back the lateral walls of the openings and a topside of the sacrificial layer at an etching rate sufficient to form smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer.

The Examiner has referred to Palm et al. as disclosing every limitation of claims 1 and 4 of the instant application. However, the Examiner has not taken into account the sequence of the fabricating steps. The claims of the instant application cannot be read literally onto the method of Palm et al. since the devices of Palm et al. are trench transistor structures, which differ substantially from the products produced by the method of the invention of the instant application.

In conjunction with the limitation "forming an oxide region in each case on a side of the doped regions remote from the semiconductor body," the examiner has cited the text in column 5, lines 8-46 of Palm et al. There are only three oxide regions mentioned in this text: the oxide layer 13, which is not required for the formation of the memory cell and is therefore removed in the region of the memory cell field; the hard mask 16 for electrical isolation of the bit line stacks; and the sidewall spacers 17. Only oxide regions 16 or 17 can be meant to correspond to the relevant limitation of the claims of the instant application. However, they are not comparable to the oxide region (6) according the method of the instant application because the oxide region (6) is produced after the application of the lower boundary layer (3) and the storage layer (4), whereas the corresponding layers of Palm et al. can only be applied after the hard mask 16 and the spacers 17.

In conjunction with the limitation of applying a sacrificial layer, the text cited by the Examiner (column 5, line 47 to column 6, line 59 of Palm et al.) mentions only one sacrificial layer in the first paragraph in column 6. This sacrificial layer is used in the implantation step that takes place before the lower boundary layer 5 is applied.

In the next method step of the invention of the instant application, openings are produced in the sacrificial layer and in the layers underneath down onto the semiconductor body. The trenches 28 in Palm et al., which are cited by the examiner as the corresponding openings, are produced before the application of the lower boundary layer, the memory layer, and the sacrificial layer. Therefore, the trenches 28 of the method of Palm et al. cannot be identified with the openings that are produced in the sacrificial layer according to the invention of the instant application. The sacrificial layer of Palm et al. cited by the examiner is removed before the application of conductively doped polysilicon 18 into the trenches. In the method of the invention of the instant application, the sacrificial layer is removed after the introduction of polysilicon into the openings. In contrast to the method of the invention of the instant application, when in Palm et al.'s method the polysilicon is applied as material of the gate electrodes, the upper boundary layer 7 is already present. The polysilicon is oxidized to regions 29 above the gate electrodes in the method of Palm et al. According to FIG. 4.3a of Palm et al., which shows a sequel of the process in this variant, the oxidized regions 29 are removed before the layer sequence for the word lines 32 is applied. In contrast, the oxide regions (6) that are produced by the

method of the invention of the instant application are electric insulations of the final product.

There is even more difficulty to read independent claim 4 of the instant application on the method described by Palm et al., since the etching of smooth sides on the sacrificial layer, the storage layer, and the lower boundary layer cannot be found in Palm et al. The Examiner has identified the openings with the trenches 28 of Palm et al. However, there is no etching step to produce smooth sides of the trenches after the application of the lower boundary layer, the storage layer, and the sacrificial layer.

There is no variant of the method described by Palm et al. that includes all the limitations of either claim 1 or claim 4 of the instant application. Since the production steps themselves belong to standard semiconductor technology, accidental coincidences between single steps or short sequences of production steps of different methods have to be expected. As the analysis by individual limitations viewed in their coherence shows, the methods of the independent claims 1 and 4 of the instant application are substantially different from the methods disclosed by Palm et al. The inventive methods of the instant application would not have been obvious from Palm et al. because the devices produced are fundamentally different.

The method according to the invention of the instant application produces a planar device, not a trench device. There is no indication in Palm et al. how single production steps could have been separated, modified, and rearranged in a way to arrive at the method of the invention of the instant application, which solves a specific problem that did not occur in the devices produced with Palm et al.'s method.

It is accordingly believed to be clear that Palm et al. do not show or suggest the method according to claims 1 or 4 of the instant application. Claims 1 and 4 are, therefore, believed to be patentable over Palm et al. and since all of the dependent claims are ultimately dependent on claims 1 or 4, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-7 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is merely a correction of a typographical error and it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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